In the claims:

1. (currently amended) A computer system for transferring ~~messages~~ data between a receiving central processing unit (CPU) and a transmitting CPU by using only write operations therebetween for the purpose of avoiding a direct read operation ~~between said receiving CPU and said~~ by the transmitting CPU from the receiving CPU, said system comprising:

a) at least one receiving central processing unit (CPU) comprising at least a read head register, a first queue length register, and a first total read register;

b) at least one transmitting CPU comprising at least a write head register, a second total read register, a total write register, and a second queue length register;

c) a local memory for said receiving CPU;

d) a local memory for said transmitting CPU;

e) means for connecting between said receiving CPU and said transmitting CPU where such means transfers write operations faster than read operations; ~~and~~

f) a circular queue defined between designated addresses in said local memory of said receiving CPU, wherein said read head register contains a pointer to the location of the next read from said circular queue and said write head register contains a pointer to the location of the next write into said circular queue;

g) means for periodically updating said second total read register with the content of said first total read register; and

h) means for adding and updating at least a message separator between messages, ~~wherein~~ such that said transmitting CPU performs a read operation ~~of~~ from said receiving CPU ~~is achieved when said transmitting CPU performs~~ by the performance of:

1) a write operation providing a separator to said local memory of said receiving CPU at a location pointed to by said write head register; ~~and~~

2) a write operation of at least one message to said local memory of said receiving CPU at a location pointed to by said write head register, requesting data to be read by said transmitting CPU, and

3) a write operation performed by said receiving CPU to said transmitting CPU containing said data to be read by said transmitting CPU.